AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1-13. (Cancelled)

14. (Previously Presented) An architecture for a data storage device, comprising:

a first data storage device control circuit that includes a first input/output (I/O) interface; and

an application circuit including a buffer that stores application data and data storage device control data, a mapping driver that maps logical addresses to physical addresses, and a second I/O interface that communicates with at least one of said buffer and said mapping driver, wherein said physical addresses and data are transmitted by said second I/O interface to said first I/O interface,

wherein said first data storage device control circuit includes a data storage device controller (DSDC), a data storage device processor, a spindle motor driver, a read/write arm driver, and a read channel driver, wherein said DSDC communicates with said first I/O interface and with at least one of said data storage device processor, said spindle motor driver, said read/write arm driver, and said read channel driver, wherein said application circuit includes at least one of an application specific integrated circuit (ASIC) and an application processor that communicates with said buffer, wherein at least one of said application processor and said ASIC sends a data request to said mapping driver, wherein said mapping driver periodically receives at least one of head location and sector location status from said DSDC, and wherein said mapping driver sends an estimated response time for said data request to said at least one of said application processor and said ASIC.

15. (Original) The data storage device architecture of claim 14 wherein said at least one of said application processor and said ASIC schedules at least one task that is not data access related before said estimated response time elapses.

16-54. (Cancelled)

55. (Previously Presented) An architecture for a data storage device, comprising:

a data storage device control circuit that includes a first input/output (I/O) interface; and

an application circuit including a buffer that stores application data and data storage device control data, a mapping driver that maps logical addresses to physical addresses, a data storage device controller (DSDC), and a second I/O interface that communicates with at least one of said DSDC, said mapping driver and said buffer, wherein:

data to be stored on the data storage device and data storage device control signals including at least one of read/write arm position data and spindle control data are transmitted by said second I/O interface to said first I/O interface;

said data storage device control circuit includes at least one of a spindle motor driver, a read/write arm driver, and a read channel driver that communicate with said first I/O interface;

said application circuit includes at least one of an application specific integrated circuit (ASIC) and an application processor that communicates with said buffer;

at least one of said application processor and said ASIC sends a data request to said mapping driver;

said mapping driver periodically receives at least one of head location and sector location status from said DSDC; and

said mapping driver sends an estimated response time for said data request to said at least one of said application processor and said ASIC.

56. (Original) The data storage device architecture of claim 55 wherein said at least one of said application processor and said ASIC schedules at least one task that is not data access related before said estimated response time elapses.

57-72. (Cancelled)

73. (Previously Presented) An architecture for a data storage device, comprising:

first control means for controlling the data storage device and that includes first interface means for providing an input/output interface for said first control means; and application means for providing application functionality and including buffer means for storing application data and data storage device control data, mapping means for mapping logical addresses to physical addresses, and second interface means for providing an input/output interface for said application means and for communicating with at least one of said buffer means and said mapping means, wherein:

said physical addresses and data are transmitted by said second interface means to said first interface means;

said first control means includes data storage device controller (DSDC) means for providing data storage device controller functions, data storage device processing means for performing data storage device processing functions, and driving means for providing at least one of a spindle motor driver, a read/write arm driver, and a read channel driver;

said DSDC means communicates with said first interface means and with at least one of said data storage device processing means and said driving means;

said application means includes application processing means for performing application processing and for communicating with said buffer means;

said application processing means sends a data request to said mapping means;

said mapping means periodically receives at least one of head location and sector location status from said DSDC means; and

said mapping means sends an estimated response time for said data request to said application processing means.

74. (Original) The data storage device architecture of claim 73 wherein said application processing means schedules at least one task that is not data access related before said estimated response time elapses.

75-113. (Cancelled)

114. (Previously Presented) An architecture for a data storage device, comprising:

first control means for controlling the data storage device and that includes first interface means for providing an input/output interface for said first control means; and

application means including buffer means for storing application data and data storage device control data, mapping means for mapping logical addresses to physical addresses, data storage device controller (DSDC) means for providing data storage device controller functions, and second interface means for providing an input/output interface for said application means and for communicating with at least one of said DSDC means, said mapping means and said buffer means, wherein:

data to be stored on the data storage device and data storage device control signals including at least one of read/write arm position data and spindle control data are transmitted by said second interface means to said first interface means;

said first control means includes driving means for providing at least one of a spindle motor driver, a read/write arm driver, and a read channel driver that communicates with said first interface means;

said application means includes application processing means for performing application processing functions and for communicating with said buffer means;

said application processing means sends a data request to said mapping means;

said mapping means periodically receives at least one of head location and sector location status from said DSDC means; and

said mapping means sends an estimated response time for said data request to said application processing means.

115. (Original) The data storage device architecture of claim 114 wherein said application processing means schedules at least one task that is not data access related before said estimated response time elapses.

116-125. (Cancelled)

126. (Previously Presented) A method for operating a data storage device, comprising:

storing application data and data storage device control data in a buffer associated with an application circuit;

mapping logical addresses to physical addresses using said application circuit;

transmitting said physical addresses and data from said application circuit to a data storage device circuit;

sending a data request using said application circuit;

periodically receiving at least one of head location and sector location status data from said data storage device control circuit; and

estimating a response time for said data request from said head location and sector location status data.

127. (Original) The method of claim 126 further comprising scheduling at least one task that is not data access related before said estimated response time elapses.

128-158. (Cancelled)

159. (Previously Presented) A method for providing an architecture for a data storage device, comprising:

storing application data and data storage device control data in an application circuit;

mapping logical addresses to physical addresses using said application circuit;

transmitting data to be stored on the data storage device from said application circuit to said data storage device control circuit;

transmitting data storage device control signals including at least one of read/write arm position data and spindle control data from said application circuit to said data storage device control circuit;

generating a data request using said application circuit;

periodically monitoring at least one of head location and sector location status using said application circuit; and

generating an estimated response time for said data request.

160. (Original) The method of claim 159 further comprising scheduling at least one task that is not data access related before said estimated response time elapses.

161-174. (Cancelled)

175. (Previously Presented) A processor chipset that communicates with a data storage device, comprising:

an input/output (I/O) circuit that provides an I/O interface for at least one of serial, audio, basic input/output system (BIOS), local area network, mouse, and keyboard connections and that includes:

a mapping driver that maps logical addresses to physical addresses;

a data storage device controller (DSDC) that communicates with said mapping driver and that controls the data storage device; and

a first I/O interface that communicates with at least one of said DSDC and said mapping driver, wherein data to be stored on the data storage device and data storage device control signals including at least one of read/write arm position data and spindle control data are transmitted by said first I/O interface to the data storage device; and

a processor that performs at least one of data and control processing and that communicates with said I/O circuit, wherein said processor sends a data request to said mapping driver, wherein said mapping driver periodically receives at least one of head location and sector location status from said DSDC, and wherein said mapping driver sends an estimated response time for said data request to said processor.

176. (Original) The processor chipset of Claim 175 wherein said processor schedules at least one task that is not data access related before said estimated response time elapses.

177-190. (Cancelled)

191. (Previously Presented) A processor chipset that communicates with a data storage device, comprising:

processor chipset input/output (I/O) means for providing an I/O interface to said processor chipset for at least one of serial, audio, basic input/output system (BIOS), local area network, mouse, and keyboard connections and that includes:

mapping means for mapping logical addresses to physical addresses;

data storage device controller (DSDC) means that communicates with said mapping means for controlling the data storage device; and

first I/O interface means for communicating with at least one of said DSDC means and said mapping means, wherein data to be stored on the data storage device and data storage device control signals including at least one of read/write arm position data and spindle control data are transmitted by said first I/O interface means to the data storage device; and

processing means that communicates with said processor chipset I/0 means for performing at least one of data and control processing,

wherein said processing means sends a data request to said mapping means, wherein said mapping means periodically receives at least one of head location and sector location status from said DSDC means, and wherein said mapping means sends an estimated response time for said data request to said processing means.

192. (Original) The processor chipset of Claim 191 wherein said processing means schedules at least one task that is not data access related before said estimated response time elapses.

193-195. (Cancelled)